CLAIMS

1. An apparatus comprising:

one or more look-up-tables (LUTs) configured to provide logical functions, wherein said one or more LUTs are implemented within a multiport memory.

2. The apparatus according to claim 1, wherein said multiport memory comprises a dual port memory.

3. The apparatus according to claim 1, wherein said multiport memory comprises a quad port memory.

4. The apparatus according to claim 1, wherein said multiport memory is selected from a group consisting of a RAM, a ROM, a PROM, an EPROM, an EEPROM, a flash memory and other appropriate types of memories.

5. The apparatus according to claim 1, wherein each of said one or more LUTs is configured to receive one or more inputs.

6. The apparatus according to claim 5, wherein each of said one or more inputs comprise single-bit or multi-bit input in a serial or parallel configuration.

7. The apparatus according to claim 5, wherein each of said one or more LUTs is further configured to generate a partial product signal.

8. The apparatus according to claim 8, wherein each of said one or more LUTs is further configured to present said partial product signal in response to said one or more inputs.

9. The apparatus according to claim 8, further comprising an adder circuit configured to receive said one or more partial product signals and present an output.

10. The apparatus according to claim 9, wherein said adder is further configured to present said output in response to one or more second signals.

11. The apparatus according to claim 10, further comprising a routable interconnect.

12. The apparatus according to claim 1, further comprising:

one or more register configured to increase a throughput of said one or more look-up-tables.

13. The apparatus according to claim 1, wherein said logical functions comprise arithmetic functions and other logic functions.

14. An apparatus comprising:

means for providing one or more look-up-table (LUTs) in a multiport memory; and

means for providing one or more logical functions, in response to said one or more LUTs, to at least one port of said multiport memory.

15. A method for implementing logical functions, comprising the steps of:

(A) providing one or more look-up-tables (LUTs) in a multiport memory; and

(B) providing one or more logical functions, in response to said one or more LUTs, to at least one port of said multiport memory.

(5) apparatus 14→15

16. The method according to claim 14, wherein said multiport memory comprises a dual port or quad port memory.

17. The method according to claim 14, further comprising:

receiving one or more input signals, each comprising a single-bit or multi-bit input in a serial or parallel configuration.

18. The method according to claim 14, wherein said memory is selected from a group consisting of a RAM, a ROM, a PROM, an EPROM, an EEPROM, a flash memory and other appropriate types of memory.

19. The method according to claim 14, further comprising the steps of:

(C) presenting one or more partial product signals; and

(D) adding said one or more partial product signals.

20. The method according to claim 14, wherein step (D) is further configured in response to one or more shift signals.